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of the Invention The present invention relates generally to a method for fabricating semiconductor devices, and more particularly, to a method for fabricating a flash memory cell. 2. Description of the Related Art In a flash memory cell, the source area is covered with a block stack and the drain area is not covered with the block stack. In a flash memory device using such a structure, the block stack of a memory cell in an erase state has a small step height due to the limited focus depth of an ion implantation process, and thus has a step difference in height therebetween and a step difference in height between the memory cell area and the surrounding areas. As the height of the step difference increases, the electric field is increased and the quality of an interface between the block stack and an ONO layer deteriorates. In addition, if the height of the step difference between the memory cell area and the surrounding areas is small, the ONO layer is formed thickly and thus the cell coupling factor is reduced. Further, if the height of the step difference between the memory cell area and the surrounding areas is large, the height difference between the ONO layer and the ONO of the memory cell becomes large. As a result, the reliability of the ONO layer deteriorates. On the other hand, if the height of the step difference between the memory cell area and the surrounding areas is small, the distance between the floating gate and the drain is increased and thus the gate coupling factor is reduced. Further, if 3e33713323

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